Palacký University Olomouc

REGIONAL CENTRE OF ADVANCED TECHNOLOGIES AND MATERIALS

MINISTRY OF EDUCATION, YOUTH AND SPORTS

PURCHASE CONTRACT No. 189/0021/RI/2015

I. CONTRACTING PARTIES:

BUYER:	**PALACKÝ UNIVERSITY IN OLOMOUC**
Office:	Křížkovského 8, 771 47 Olomouc, Czech Republic
Rector:	Mgr. Jaroslav Miller, M.A., Ph.D.
Person authorized to act in technical matters:	RNDr. Petr Schovánek
Ident. no.:	61989592
Tax Ident. no.:	CZ61989592
Bank contact:	Komerční banka, a.s. Branch in Olomouc, Czech Republic Account no.: 19-1096330227/0100

(hereinafter referred to as "Buyer")

and

SELLER:	***Schmitt Europe Ltd.***
Office:	*2 Leofric Court, Coventry CV3 2NT, United Kingdom*,
Registration in Companies Register:	*3202316*,
Statutory body:	*Companies House UK*,
Person authorized to act in contractual matters:	*Mr Jonathan Atkinson*,
Person authorized to act in technical matters:	*Mr Christian Staats*,
Ident. no.:	*670026757*,
Tax Ident. no.:	*GB670026757*,
Bank contact:	*HSBC plc, 27-32 Poultry, London EC2P 2BX*,
Account no.:	*IBAN: GB40MIDL40051557292118, BIC:MIDLGB22*,

(hereinafter referred to as "Seller")

are closing on the bellow stated day, month and year according to provision of Section 2079 of the Act no. 89/2012 Coll., Civil Code, as amended this purchase contract (hereinafter referred to as "Contract").

The Buyer and the Seller enter into this Contract due to the fact that the Seller's bid for delivery of the subject of performance hereof has been selected by the Buyer as the best bid in the tender called „System for evaluation and analysis of scatter data" prior to entering into this Contract.

II. Subject of the fulfillment

1. The Seller undertakes, under this contract, to deliver to the Buyer the System for evaluation and analysis of scatter data, together with all the accessories (hereinafter referred to as the "Goods")

and the technical specifications mentioned in the Seller's offer dated 09.07.2015, that is an integral part of this contract as its Annex No. 1. The seller is not entitled to deliver goods in larger quantity as stated in § 2093 Civil Code. Both parties to this contract agreed that the application of provision § 2099(2) Civil Code be excluded and thus will not apply.

2. The Seller hereby undertakes to surrender the Goods specified in Annex no. 1 to this Contract to the Buyer and allow him to acquire title to it, provide the warranty service under the conditions stipulated by this contract.

3.The Buyer agrees to take over the Goods and pay the seller the purchase price in the way and on the day agreed in this Contract.

4. The Seller declares pursuant to Section 2103 Civil Code, that the Goods is without any faults or defects.

5.The Goods shall be fully functional without any additional costs or expenditures necessary to be paid by the Buyer.

III. Term and place of delivery

1. The Seller undertakes to deliver the goods to the place of delivery within 5 weeks from the date of signing the purchase contract by both parties.

2. Place of delivery: Regional Centre of Advanced Technologies and Materials, Division of Optical and Photonic Technology, Faculty of Science of UP in Olomouc, 17. listopadu 50a, 771 46 Olomouc, Czech Republic. Person authorised to take over the delivery on the basis of a handover protocol: RNDr. Petr Schovánek, or a person authorised by him to take over the goods.

3. Both parties agreed, that Section 2129 and Section 2127 Civil Code on self-help sale will be excluded and thus shall not be applicable in the case of delay in take-over of the Goods by the Buyer.

IV. Purchase price

1. The purchase price is set by an agreement of the contracting parties under this contract the purchase price of EUR €33,125.00 without VAT.

2. The purchase price covers all the costs related to the supply of the goods (in particular the transport to the place of delivery, insurance, customs duties, fees, licence fees and copyrights, warranty service) as well as profit of the seller connected with the delivery.

3. The purchase price is set as a fixed price, the highest acceptable and maximal, covering all the costs related to the supply of the goods.

4. The seller takes the responsibility for the fact, that the VAT rate at the time of invoicing is stipulated in compliance with the legislation.

V. Payment terms

1. The payment for the supply will be made on the basis of a due tax document (invoice) containing all relevant particulars, within a maturity date of 30 days following the day of its delivery to the Buyer. The invoice will be issued by the Seller not sooner than after delivery of the goods, delivering the documents required by law, relevant documentation and instruction to use, perform acceptance tests. The document on a due fulfillment of obligations by the Seller specified in the preceding sentence is a dated handover protocol signed by authorized persons of both contracting parties.

2. The invoice issued by the Seller must include all tax document prerequisites in accordance with Act No. 235/2004 Coll. on value added tax as amended and the prerequisites of a commercial deed pursuant to Section 435 of the Civil Code as well as identification of the contract, on the basis of which the fulfilment has been provided. The Seller shall affix the invoice with the stamp and signature of the person authorised to issue the invoice and with the project name and registration number, including number of this Contract.

3. If the invoice issued by the Seller does not contain any of the obligatory particulars or if the Seller incorrectly invoices the price or the VAT, the Buyer is entitled to return such invoice to the Seller before the expiration of its maturity date for the correction, stating the reason of its returning. The Seller shall correct it by issuing a new invoice. The initial maturity date stops running on the day of sending the incorrect invoice to the Seller and a new maturity day starts running on the day of the delivery a new invoice to the Buyer.

4. The contracting parties agree that the obligation to pay the purchase price is fulfilled on the day when the given sum is sent from the Buyer's account to the Seller's account given above in this contract.

5. The Seller declares, that he takes the risk of Clausula rebus sic standibus pursuant to Section 1765(2) of the Civil Code and Section 1765(1) and Section 1766 of the Civil Code is excluded and thus inapplicable.

VI. The Seller´s responsibility for defects

1. The Seller provides to the Buyer a warranty for the quality of the Goods according to § 2113 and follow. Civil Code within the period of 12 months since the day of signing the protocol according to article V(1) of this contract.

2. During the guaranty period, the respective defects shall be removed within 30 calendar days at the latest after the day of the start of the defect notification (by email, letter form, fax), unless otherwise agreed in writing by persons authorized by contracting parties for technical matters. The seller is obliged to provide repairs in the place of delivery. Shall that be technically impossible, the seller shall take over the device in order to repair it after signing a written record stating suggested procedure agreed by the person authorised to act in technical matters for the contracting person. The contracting parties have agreed that § 2110 Civil Code shall not apply. The buyer is entitled to withdraw from the contract for the defects or to require the delivery of new goods irrespective of the fact that the goods might be returned to the seller or possibly return the goods in the quality as it was received by the buyer.

3. If any defects are found during the guaranty period, the Buyer is entitled to inform the Seller in a demonstrable way about the defects. The defects announced to the Seller during the guaranty period shall be removed by the Seller free of charge.

4. **The conditions of the complete acceptance and handover of the good ("acceptance tests"):**

a) Measurement of reference sample with known parameters, accomplishment of control calculation of BSDF function, roughness parameter R_q and PSD function. The results must be in tolerance ±5% with respect to reference results.

b) Communication test with given scatterometer, check of function

c) Data evaluation of previously taken measurements from given scatterometer to the extent to article a).

d) Fulfillment of all technical parametres required by the contracting person.

The above mentioned tests are condition of the handover of the goods by buyer.

VII. Contractual penalty

1. In the case of Seller's delay with delivery of any part of the Goods according to the period stated in the section III.(1) of this Contract, the Buyer will be entitled to a contractual penalty amounting 10,- EUR without VAT for each started day of the delay with its delivery.

2. The seller undertakes to pay to the buyer contractual penalty amounting to 10,- EUR without VAT for each starting day after the lapse of time for repair in the warranty period in compliance with this contract for each particular case.

3. The parties have agreed that arranging the contractual penalty pursuant to this Section does not affect the right of the Buyer for the compensation of the damages arisen from the breach of the duty strengthened in VI(1) of this Contract. That means that contractual parties have agreed on exclusion of application of Section 2050 Civil Code.

4. The maturity date of the charged contractual penalties is 30 days from the day of delivery of their written statement to the given contracting party and the day of payment means the day of debiting the contractual penalty from the account of the given contracting party to the account mentioned in the statement of the contractual penalty.

5. The Buyer is entitled to include the contractual penalties in the Seller's claim of the purchase price according to § 1982 and follow. Civil Code.

VIII. Final provisions

1. The Buyer reserves the right to publish the contents of the concluded Purchase Contract.

2. The contracting parties expressly agreed that all the rights and obligations under this contract, as well as the rights and obligations arising from this contract, will be settled in accordance with the appropriate provisions of the code no. 89/2012 Coll., Civil Code and the Czech law system.

3. The provisions of this contract are separable. If any part of an obligation under this contract is or becomes invalid or non-enforceable, this shall not affect the validity and the enforcement of other obligations under this contract and the contracting parties undertake to replace such invalid or non-enforceable part of obligation with a new, valid and enforceable part of the obligation, the subject of which will correspond at the best to the subject of the original obligation. If the contract does not contain a provision which would be justifiable for the determination of the rights and obligations, the contracting parties will make all the efforts to implement such provision in the contract.

4. The contracting parties may modify or complete this contract only in the form of written amendments numbered in the increasing order, expressly declared as amendments to this contract and signed by the authorized representatives of the contracting parties.

5. The Buyer is entitled in accordance with § 2001 Civil Code to withdraw from this contract for its substantial breach by the Seller; the substantial breach means:

- the delay of the contractually determined term of delivery of the subject of the contract by more than 20 days,
- a failure to observe the technical specifications of the goods mentioned in the Seller's offer.
- delay of the seller in repairing and removing the defects by more than 10 days.

The withdrawal from the contract shall be made in a written form and becomes effective on the day of the delivery of the written notice to the other contracting party.

6. The Seller is not entitled to cede his rights and obligations under this contract to a third person without the Buyer's approval.

7. This Purchase Contract becomes effective on the day of its signature by both contracting parties.

8. This Purchase Contract is made in five copies considered as originals, signed by the authorized representatives of the contracting parties; the Buyer will obtain three copies and the Seller will obtain two copies.

9. The following Annexes form an integral part of this Purchase Contract:
Annex 1 – Seller's offer dated 9th July 2015 ref B3922

In Olomouc, on 13.8.2015

UNIVERZITA PALACKÉHO v OLOMOUCI
rektorát
Křížkovského 8, 771 47 Olomouc

prof. Mgr. Jaroslav Miller, M.A., Ph.D
rector

In Coventry, UK, on 09.07.2015

Schmitt Europe Ltd
Ground Floor Unit 2
Electric Court Progress Way
Tollgate Industrial Estate
Coventry CV3 2NT
Tel: 0044 (0)2476 651774
Fax: 0044 (0)2476 450456

Mr Jonathan Atkinson
Company Secretary

Tender No. B3922

DYNAMIC BALANCE SYSTEM
A PRODUCT LINE OF SCHMITT INDUSTRIES, INC.

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Palacky University in Olomouc
Krizkovskeho 8
771 47 Olomouc
Czech Republic

Date: 9-7-2015

ORIGINAL

Attn. of: prof. Mgr. Jaroslav Miller, M.A., Ph.D
Ident. No.: 619 89 592
Tax Ident. No.: CZ 619 89 592

Schmitt contacts: Jon Atkinson / Bill Craddock
Tel: +44 2476 651774
Email: jon@schmitt.co.uk / bill@schmitt.co.uk

Scope / Description:

To supply and warranty a System for evaluation and analysis of scatter data for 'CASI Scatterometer'

Technical Specification:
The Schmitt system is designed to evaluate photodiode / photomultiplier light scattered from optical materials.
The system includes MS Windows 7 software and a PCI card for a personal desktop computer.
The PCI card communicates with the motion controller / receiver / lock in amplifier of the scatterometer.
The software allows for Obtaining, Analyzing, Evaluating and Storing the measured data. The software also allows the data be recalled and can calculate the properties of the scattered light to determine particular optical and mechanical parameters of the tested material.
The software stores the measured data as BSDF values and can calculate the parameters of the scattered light field like BSDF (BTDF, BRDF), CTIS and PSD, Rq.
Measurement of a reference sample with known parameters and the control calculation of BSDF, Rq and PSD should be within +/-5% tolerance of the reference results.
The system is able to multi-task, and it is possible to purchase additional licenses for remote computers to be able to view and analyze data.
The software and PCI card are fully compatible with the CASI scatterometer and its photometric devices.
PCI card features include:
5 volt signal slot, 2 off – 37 pin D sub connections to communicate to CASI with on board EEPROM, 2Kx16, 93CS66LM8.
PLX PCI interface PCI9030 in a TQ176 IC package. A Nippon Pulse America STEP Motor controller PCL240MS. Xilinx CPLD XC95144-15PQ160C.
Installation assistance by email and telephone/fax is available if required.
Complete documentation of the system and a declaration of conformity are included in this tender in English language.

Detailed interface and communication protocol is given on pages 2, 3 and 4 of this tender and match the specification as detailed in Annex 4.

Price (valid until 30.11.2015):

To supply and warranty a System for evaluation and analysis of scatter data for 'CASI Scatterometer' as described above and detailed on pages 2, 3 and 4 of this document. **Total exc. VAT: €33,125.00**

Terms:

As detailed in Annex 3 attached to this offer.

WCraddock

Signed: B Craddock – Sales Manager

Schmitt Europe Ltd
Ground Floor Unit 2
Leofric Court Progress Way
Binley Industrial Estate
Coventry CV3 2NT
Tel: 0044 (0)2476 651774
Fax: 0044 (0)2476 450456

Jon Atkinson – Company Secretary

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Technical Specifications and Notes:

1) Card type
   a) **Universal PCI (can be plugged into 3.3V or 5V PCI signal slots). Can be usable in all PCI products
   b) 5V signal PCI slot.
2) Motor Controller Components used
   a) 40 pin dip through hole part
3) **PCL-240MS - 44 pin PLCC surface mount. BASIC OPERATION MODE is set to 0 in all existing software. PCL-240K is the original chip used in the Interface/Controller design.
4) I/O Compatibility
   a) Compatible with existing addresses (32 words)
   b) Optional new address space using fewer bytes
5) ADC Components used
   a) 40 pin dip through hole part
6) **CS5014-BL14 - 44 pin PLCC surface mount.
7) External connectors
   a) like existing, PCI slot brackets, internal cables
   b) **new cabling, 2 PCI slots brackets, one internal cable
   c) external cable adapters, 1 PCI slot
8) Informational
   a) Multi-layer boards required to meet PCI signal impedance spec.
   b) Plated finger connectors on PC card
9) Component sizes
   a) 1206
   b) **0805

ADC Function

a) **Clock:** The clock is asynchronous to the bus timing. The clock will be near 2 MHz The original board ran at 2 MHz. Min lo duty cycle: 40%. Min hi duty cycle: 40%. The chip can operate at up to 4 MHz
b) **Data Delay:** The data delay is negligible because a software delay is required. It is a max of 100 ns from end of conversion to data availability.
c) **Read Cycle:** Min A0, INTRLV setup to CS and RD: 20 ns. Min access CS lo and RD lo to data valid: 120 ns. Max CS hi or RD hi to data float: 110 ns. Min CS hi or RD hi to A0 invalid or INTRLV invalid: 50 ns.
d) **Write Cycle:** The chip has no write cycle. The write cycle will generate a HOLD pulse instead of a write pulse. Min HOLD pulse lo time: 550 ns (at 2 MHz), 531 ns at 2.1 MHz.
e) **Reset Cycle:** After reset about 750 ms are required before the chip is calibrated. Simultaneously asserting HOLD, CS, and A0 low will also cause a calibration cycle which requires 750 ms to complete. EOC (End of cycle) will be asserted at the end of calibration.
f) **Logic:** All connecting logic previously provide in SSI on the 755101 will be provided in the CPLD.
g) **Timing:** All clock, read, and HOLD timing will be provided by the combined designs of the PCI registers and the CPLD.

I/O MAP

h) **Compatibility: The I/O map must exactly match the 755-101 board for register access**. The only exception is for signals that were never used in any applications. It turns out that if the signals weren't in the two 37 pin connectors then they were never used. The 755-115 is designed to have all the pins in the original 37 pin connectors and no more. Extra spaces in the map can be used to activate driver functions if needed.
i) **Timing:** The second mapping function eases the timing requirements by making the best use of the programmable timing features in the PCI chip. Three separate devices require different timing: The motor controller chip, the ADC chip, and the registers internal to the CPLD. The CPLD registers can be made synchronous and are fast enough that they can borrow the timing of the other chips where needed.
j) **Address:** The normal base I/O address of the 755-101 was 0x340 to 0x35F (32 bytes). CASI was fixed at this address. TASC and SRL software allowed different jumper selections on natural 32 byte boundaries. The 755-115 will use a driver to set the address, but CASI software still needs the fixed address locations.
k) **Offsets:** The following table shows the functions and their mappings with respect to PCI Local Address Space (AS). The PCI chip select timing will be different for each, optimized for each range.

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PCI CHIP NOTES

Slave: It is slave only and requires extensive polling for high speed throughput. It can generate interrupts, but this capability is not used by DOS programs. A future Windows driver could use the interrupt capability to get high I/O speed without using resources like polling does.

Timing: See timing.sch for local bus timing diagrams. Timing is coordinated with the CPLD to get the final results. Because the CPLD will generate read and write strobes to the motor controller and ADC, and to make the logic as simple as possible, burst mode will not be disabled, allowing the RD# and WR# to assert and deassert only once per memory byte cycle. READY# is disabled so that only wait states in the PCI9030 control the timing. The software should only be using single byte read and write instructions. Specific timing information is in the CPLD section for each signal.

Power: Power calculations are in power.xls. All consumed is dissipated. No difference between D0 and D3 unless clock is stopped.

Registers: The PCI9030 configuration registers must be set up as follows from the EEPROM. All unused or unspecified bits must be set to 0. P – PCI Configuration Register, L – Local Configuration Register, E – Location in EEPROM. Addresses and Values in Hex.

CPLD CHIP NOTES

Note that throughout the following descriptions the signal name NAME implies assertion and !NAME implies not assertion. **RD#** is asserted lo and not asserted hi: RD implies asserted (lo), !RD implies not asserted (hi). **A0** is asserted hi and not asserted lo: A0 implies asserted (hi),!A0 implies not asserted (lo).

CLOCK: This input is also the local clock for the synchronous PCI9030 timing. The clock will be 25 MHz, 40% to 60% duty cycle. This gives a 40 ns period on the local bus.

Address and Data: The internal address bus is defined from the address input lines.

A0, A1: To aid in timing, the address lines to the motor controller and ADC chips will be latched, using the ADS signal as a strobe. This keeps these lines stable for at least one cycle after each memory cycle has ended, satisfying address hold times. While the PCI9030 provides a means to keep the address lines stable after WR is deasserted, it does not provide for a way to keep them stable after RD is deasserted.

CLK_5MHZ: This clock is derived from CLOCK. The output toggles at 2 and 3 CLOCK cycles alternately, giving a 40% / 60% duty cycle. The minimum hi is 2 cycles or 80 ns.

MTR_RD: With simple logic this asserts at least 30 ns (40 ns nominal, 0 ms min) after A0, A1 become stable (RSD = 0). The normal RD strobe from the PCI9030 is nominally 40 ns which is sufficiently greater than the 24 ns minimum. CPLD delays and motor controller access time require that one clock be added to the data cycle (NRAD=1). To keep the address from changing before the rising edge of MTR_RD, a clock is added at the end of the cycle (NXDA=1). This signal is decoded in Local I/O Space 0.

MTR_WR: With simple logic this asserts at least 30 ns (40 ns nominal, 0 ms min) after A0, A1 become stable (WSD = 0). The normal WR strobe from the PCI9030 is nominally 40 ns which is greater than the 33 ns minimum. However skew delays between signals and transitions may make up the 7 ns difference between the two times. Adding a one clock address to data cycle (NWAD=1) guarantees the minimum time. MTR_WR is delayed from WR by the CPLD causing it to go high after the data lines. Adding a one clock Write Cycle Hold (WSH=1) extends the data stability beyond to rising edge of MTR-WR. One clock is added to the end of the cycle (NXDA=1) for MTR_RD that applies to both read and write. This signal is decoded in Local I/O Space 0.

CLK_2MHZ: This clock is derived from CLOCK. The output toggles every 6 CLOCK cycles, giving a 50% /50% duty cycle. The frequency is actually 25/12 = 2.1 MHz.

ADC_RD: With simple logic this asserts at least 30 ns (40 ns nominal, 20 ms min) after A0, A1 become stable (RSD = 0). Data becomes available 120 ns after ADC_RC asserts. With NRAD set to 3 the data would be available 5 to 10 ns more than the required setup time. Since this may be a little tight, use 4 clocks (NRAD=4). The data lines will not tri-state until 110 ns after ADC_RD deasserts. The next data from the PCI (cycle immediately following ADS assertion) must not be put on the bus until after the 110 ns. Waiting 3 clocks after the cycle satisfies this delay (NXDA=3). A0 and A1 must be held stable for 50 ns after ADC_RD is deasserted. This is satisfied by a 2 clock delay after the cycle (NXDA=3 already). This signal is decoded in Local I/O Space 3.

ADC_HLD: This signal is mirrored by ADC_CS during a write cycle. ADC_CS will discuss this timing. ADC_HLD must remain lo for 531 ns min. Inserting 13 clocks into the write cycle satisfies this timing (NWAD=13). Data is not involved with this signal (WCH=0). This signal is decoded in Local I/O Space 3

ADC_CS: This signal mirrors either ADC_RD or ADC_HLD. Its timing simply follows the signal it mirrors. This signal must maintain timing requirements for both read and write cycles. A0 and A1 must be stable for 20 ns prior to ADC_CS assertion (WSD=0, RSD=0). A0 and A1 must be stable for 50 ns after ADC_CS is deasserted. 2 clock delays after the cycle satisfy this requirement. (NXDA=3 for ADC_RD). This signal is decoded in Local I/O Space 3.

ADC_RST: This signal should be asserted for at least 100 ns when LRESET is asserted.

INxx Port Bits: Bits internal and external to the CPLD are passed through these ports to the data bus during the appropriate read cycles on the local bus. The individual port lines are selected for the data output lines via address decoding. The data

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output lines are gated onto the bus via output enables, also generated through address decoding. The decoding assures that the data lines are driven for all read cycles.

Space 1, Space 2: The timing for Local I/O Spaces 1 and 2 provides (possibly excess) time for read and write operations. To allow product term clocks on the write cycle the data is stretched one clock (WCH=1). To have more than 15 ns setup time for read the read is stretched by one clock (NRAD=1).

Space 0: The timing for Local I/O Space 0 is consistent with the timing of Local I/O Spaces 1 and 2. The timing for Local I/O Space 0 was generated for the Motor Controller Chip.

OUT_ENA: The output enable signal keeps most latched output signals tri-stated following a reset. The ouputs are enabled by a read at offset 18H.

OUTxx Latch Bits: The data bus is latched into several registers to control internal and external functions.

Fault Latch: The temperature fault latch is implemented in the CPLD. logic:

Motor Controller Output: The pulse and direction pins are conditioned through the CPLD. The pulse output should go low for 18 µsec following every positive transition of the pulse input. The direction output is inverted and buffered from the direction input

Home and Limits: The limit and home logic is incorporated within the CPLD. The watch-dog circuit has been eliminated. This one-shot forced the motor to stop if the processor quit accessing the motor controller.

Plus and Minus Soft limit inputs and Home Switch generate SD signals to cause ramping down. Plus and Minus Hard limit inputs generate EL signals to cause an immediate stop. SD signals force the EL signals to cause a stop after the ramp down is complete.

The time delay logic that generates the INS signal prevents the EL signals from being asserted at the leading edge of the SD signal. FDOWN is normally lo when SD is asserted, but it goes hi shortly afterward and stays that way until the deceleration is complete. Then it goes lo and gates the SD lines onto the EL lines to end the commanded motion.